	Туре	L#	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	5	shimizu near ryu.in.	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 14:35
2	BRS	L2	750	438/638.ccls.	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 14:36
3	BRS	L3	173	2 and (anti-reflect\$3 or antireflect\$3 or anti near reflect\$3)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 14:41

	Туре	L #	Hits	Search Text	DBs	Time Stamp
4	BRS	L4	25379 8	((etch\$3 or pattern\$3)) near15 ((dielectric or insulat\$3 or oxide))	IH D(1 *	2005/01/1 1 14:47
5	BRS	L5	1351	((etch\$3 or pattern\$3)) near15 ((dielectric or insulat\$3 or oxide)) near15 (anti- reflect\$3)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 16:36
6	BRS	L6	1390	((etch\$3 or pattern\$3)) near15 ((dielectric or insulat\$3 or oxide)) near15 (anti near reflect\$3)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 16:38

	Туре	L #	Hits	Search Text	DBs	Time Stamp
7	BRS	L7	321	Milita or holesi or	IH: P() •	2005/01/1 1 16:39
8	BRS	L8	16	<pre>((etch\$3 or pattern\$3)) near15 ((dielectric or insulat\$3 or oxide)) near15 (anti near reflect\$3) near15 ((via or hole\$1 or</pre>	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 16:39

	U	1	Document ID	Title	Current OR
1			US 20040259349 A1	Method of manufacturing a semiconductor device including a multi-layer interconnect structure	438/638
2			US 20040155342 A1	Semiconductor device and manufacturing method thereof	257/751 .
3				Method of forming damascene pattern in a semiconductor device	216/20
4			1/11113111114//////	Method for fabricating semiconductor device	438/710
5			US 6630397 B1	Method to improve surface uniformity of a layer of arc used for the creation of contact plugs	438/636
6			US 6593225 B1	Method of forming a stacked dielectric layer on a semiconductor substrate having metal patterns	438/623
7			US 6475918 B1	Plasma treatment apparatus and plasma treatment method	438/714

	บ	1	Do	cument	ID	Title	Current OR
8			US B1	6440640)	Thin resist with transition metal hard mask for via etch application	430/314
9		l .	US B1	6218283	3	Method of fabricating a multi-layered wiring system of a semiconductor device	438/622
10			US	616569	5 A	Thin resist with amorphous silicon hard mask for via etch application	430/314
11			US	616258	7 A	Thin resist with transition metal hard mask for via etch application	430/314
12			US	6127070	A C	Thin resist with nitride hard mask for via etch application	430/5

	U	1	Document ID	Title	Current OR
13			TIC 5700737 A	PECVD silicon nitride for etch stop mask and ozone TEOS pattern sensitivity elimination	438/636
14				Method of forming multilayered wiring	438/636
15	X		JP 10022387 A	MANUFACTURE OF SEMICONDUCTOR DEVICE	
16			KR 2002020083 A	Method for forming contact hole of semiconductor device	